What is claimed is:

1. A processor connected to a memory via a data bus, comprising an address conversion unit operable to convert at least one lower bit of an address so as to indicate a reversed position of data in the data bus, and output the converted address to the memory, when the processor performs a memory access for the data with a smaller width than the data bus,

wherein the processor is connected to the data bus in a way that data is transmitted to and from the memory in a byte order based on an endianness which is opposite to an endianness of said processor.

2. The processor according to Claim 1, further comprising a cache memory connected to the data bus in a byte order based on the endianness of the processor,

wherein the processor reads data from the memory through the cache memory in data units of the same width as the data bus.

3. The processor according to Claim 1, executing a program that defines structure data which includes data that is smaller than a basic word length, said structure data being shared between the processor and another processor of a different endianness via the memory, said data being defined in an order within the basic word length, and said order being in reverse to an order in a definition of said structure data in a program to be executed by said another processor.

4. The processor according to Claim 3, further comprising a cache memory connected to the data bus in a byte order based on the endianness of the processor,

wherein the processor reads data from the memory through the cache memory in data units of the same width as the data bus.

5. A data sharing apparatus comprising a first processor, a second processor, and a memory, said first and second processors being of different endianness,

wherein both the first processor and the second processor are connected to the memory via a data bus, in a byte order based on the endianness of the first processor.

6. The data sharing apparatus according to Claim 5, further comprising an address conversion unit operable to convert at least one lower bit of an address so as to indicate a reversed position of data in the data bus, and output the converted address to the memory, when the second processor performs a memory access for the data with a smaller width than the data bus.

7. The data sharing apparatus according to Claim 6, further comprising a transfer unit operable to control data transfer by direct memory access,

wherein, in the case where a source and a destination require data of different endianness and data with a smaller width than the data bus is to be transferred, the transfer unit reverses an order of said data within a basic word length, for the source and the destination.

8. The data sharing apparatus according to Claim 7,

wherein the transfer unit includes a conversion unit operable to convert at least one lower bit of an address of either the source or the destination so as to indicate a reversed position of the data in the data bus, and output the converted address to the memory, in the case where a source and a destination require data of different endianness and data with a smaller width than the data bus is to be transferred.

9. The data sharing apparatus according to Claim 6,

wherein the memory stores structure data to be accessed by a first processor and a second processor,

the first processor executes a first program that defines the structure data, and

the second processor executes a second program that defines structure data which includes data that is smaller than the basic word length, said data being defined in an order within the basic word length, and said order being in reverse to an order in the first program.

10. The data sharing apparatus according to Claim 9, further comprising a transfer unit operable to control data transfer by direct memory access,

wherein, in the case where a source and a destination require data of different endianness and data with a smaller width than the data bus is to be transferred, the transfer unit reverses an order of said data within a basic word length, for the source and the destination.

11. The data sharing apparatus according to Claim 10,

wherein the transfer unit includes a conversion unit operable to convert at least one lower bit of an address of either the source or the destination so as to indicate a reversed position of the data in the data bus, and output the converted address to the memory, in the case where a source and a destination require data of different endianness and data with a smaller width than the data bus is to be transferred.

12. The data sharing apparatus according to Claim 5, further comprising a cache memory connected to the data bus in a byte

order based on the endianness of the second processor.

13. The data sharing apparatus according to Claim 12, further comprising an address conversion unit operable to convert at least one lower bit of an address so as to indicate a reversed position of data in the data bus, and output the converted address to the memory, when the second processor performs a memory access for the data with a smaller width than the data bus.

14. The data sharing apparatus according to Claim 13, further comprising a transfer unit operable to control data transfer by direct memory access,

wherein, in the case where a source and a destination require data of different endianness and data with a smaller width than the data bus is to be transferred, the transfer unit reverses an order of said data within a basic word length, for the source and the destination.

15. The data sharing apparatus according to Claim 14,

wherein the transfer unit includes a conversion unit operable to convert at least one lower bit of an address of either the source or the destination so as to indicate a reversed position of the data in the data bus, and output the converted address to the memory, in the case where a source and a destination require data of different endianness and data with a smaller width than the data bus is to be transferred.

16. The data sharing apparatus according to Claim 13

wherein the memory stores structure data to be accessed by a first processor and a second processor,

the first processor executes a first program that defines the structure data, and

the second processor executes a second program that defines structure data which includes data that is smaller than the basic word length, said data being defined in an order within the basic word length, and said order being in reverse to an order in the first program.

17. The data sharing apparatus according to Claim 16, further comprising a transfer unit operable to control data transfer by direct memory access,

wherein, in the case where a source and a destination require data of different endianness and data with a smaller width than the data bus is to be transferred, the transfer unit reverses an order of said data within a basic word length, for the source and the destination.

18. The data sharing apparatus according to Claim 17,

wherein the transfer unit includes a conversion unit operable to convert at least one lower bit of an address of either the source or the destination so as to indicate a reversed position of the data in the data bus, and output the converted address to the memory, in the case where a source and a destination require data of different endianness and data with a smaller width than the data bus is to be transferred.

19. A method of sharing data in a data processing apparatus which includes a first processor and a second processor of different endianness, and a memory to which both the first processor and the second processor are connected via a data bus, in a byte order based on the endianness of the first processor, the method comprising:

a step of causing the second processor to execute a program that defines structure data which includes data that is smaller than

a basic word length, said structure data being shared in the memory, said data being defined in an order within the basic word length, and said order being in reverse to an order in a definition of said structure data for the first processor, and

a conversion step of converting at least one lower bit of an address so as to indicate a reversed position of data in the data bus, in the case where the second processor performs a memory access for data with a smaller width than the data bus.